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Xilinx Legal

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APR 2 5 2005

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XILINX, INC ATTN: LEGAL DEPARTMENT 2100 LOGIC DR SAN JOSE, CA 95124				Co. I hereby certify that it States Postal Service, addressed to the Mai transmitted to the USI	rtificate of Mailing or Transis Foc(s) Transmittal is bein with sufficient postage for fill I Stop ISSUE FEB address TO (703) 746-4000, on the	smission g deposited with the United st class mail in an envelope i above, or being facsimile date indicated below.	
04/26/2005 WABDELR3 00000113 240040 10082518				Pat Sla		(Depositor's name)	
01 FC:1501	1400.00 DA			Fot U	Show	(Signature)	
02 FC:1504	300.00 DA			April 2	25, 2005	(Dato)	
APPLICATION NO.	FILING DATE	1	TRST NAME	D INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/082,518	02/22/2002		L. Jamo	s Hwang	X-1002 US	5974	
TITLE OF INVENTION: METHOD AND SYSTEM FOR INTEGRATING CORES IN FPGA-BASED SYSTEM-ON-CHIP (SOC)							
APPLN. TYPE	SMALL ENTITY	ISSUE FEE		PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE	
nonprovisional	NO NO	\$1400		\$300	\$1700	05/31/2005	
EXAMINER		ART UNIT		CLASS-SUBCL ASS			
WHITMORE, STACY		2825		716-016000			
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·				amunt): 🗖 Individual 🖔 Co	75124	our entity Government	
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5. Change in Entity Status (from status indicated above) \$\sum_{\text{a}}\$ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. \$\text{\text{b}}\$ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).							
The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.							
Authorized Signature				Date Ap	ril 25, 2005		
Typed or printed name Kin Kanzaki			·	Registration	No. 37,652		
This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) in application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will very depending upon the individual case. Any comments on the amount of time you require to complete his form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.							

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Alexandria, Virginia

22313-1450

Inventor(s):

L. James Hwang et

Assignee: XILINX, INC.

Serial No.: 10/082,518

conf.no. 5974

Filed:

February 22, 2002

Title: Method and System for Integrating CORES in FPGA-Based System-On-Chip (SoC)

Docket No.: X-1002 US

Enclosed: Return Receipt Postcard

Fee Transmittal - Part B

Date: April 25, 2005

VIA FACSIMILE 703-746-4000

Atty/Sec: KK/pbs